Ramesh Ganapam

PhD Student – Analog/Mixed-Signal & Digital Hardware Design Engineer
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Education

Ph.D. in KFSCIS, Emphasis on Computer Engineering, GPA: 3.75/4.0 Aug 2024 - Dec 2025
Selected Courses: Shimeng Yu - Memory Devices and Circuits, Machine Learning Algorithms.
Textbooks: Shimeng Yu - Memory Devices and Circuits, Rolf et al - In-Memory Computing Synthesis and Optimization.

Ph.D. in EECS, University of Kansas, GPA: 3.8/4.0 Jan 2021 - Jul 2024
Selected Courses: Baker - Memory Circuit Design, Baker - Mixed-Signal Circuit Design, Modern Computer Architecture, Onur - Introduction to Computer Architecture, Modern Computer Architecture.
Textbooks: Jacob et al - DRAM Circuit Design: Fundamental and High-Speed Topics, Itoh - VLSI Memory Chip Design, Jacob et al - CMOS: Circuit design, layout, and simulation.

M.E. in Electrical Engineering, BITS Pilani, Pilani Campus Aug 2016 - May 2018
Selected Courses: Advanced VLSI Design, Reconfigurable Architectures.
Textbooks: Kang et al - CMOS Digital Integrated Circuits Analysis Design, Harris et al - CMOS VLSI Design A Circuits and Systems Perspective, Palnitkar - Verilog HDL A guide to Digital Design and Synthesis.

B.Tech in ECE, Affiliated to JNTU Kakinada Aug 2010 - May 2014
Selected Courses: Analog and Digital Circuit Design, Device Physics, Electronic Networks.
Textbooks: Sedra et al - Microelectronic Circuits, Alexander et al - Fundamentals of Electrical Circuits, Neaman - Semiconductor Physics and Devices: Basic Principles, Mano - Digital Logic and Computer Design.

Skills

Languages: Verilog, Verilog-A, MATLAB, Python, C/C++
Tools: Cadence Virtuoso (Schematic/Layout, DRC, LVS), LTSpice, Cross-Sim, CACTI, DRAMSpec, Rambus Power Model, Micron Power Models, ABC, Git, LaTeX
Expertise: In-Memory Computing, DRAM/SRAM/RRAM Architecture, Static Timing Analysis, Mixed-Signal and Analog Circuit Design, Logic Synthesis, Circuit Simulation and Validation

Research Interests

My research focuses on analog/mixed-signal DRAM design using LTSpice, Cadence Virtuoso, and Verilog-A. I also have research experience in hardware synthesis and one year of Verilog RTL development. I am particularly interested in roles in analog/mixed-signal and digital hardware design.

Research Experience

GRA (FIU) - Python, ABC, Advisor: Sumit Kumar Jha Aug 2024 – Present

• Modeling large-scale Digital logic on **RRAM** memory crossbars using novel **In-Memory computing** techniques such as **PATH and FLOW-based** computing using a new data structure instead of BDDs.
• Converted large digital **ISCAS-85 and EPFL arithmetic** benchmarks into a new data structure using **ABC, AIGER**, and compared their structure with ROBDD based mapping. Results showed that this new data structure is a better efficient representation for large digital circuits. We proposed **Systematic** and **Area-opt** synthesis methods to efficiently **map** the new data structure to the RRAM memory crossbar.

GRA and GTA (KU) - Cadence Virtuoso, Advisor: Mohammad Alian (Cornell) Jan 2023 – Aug 2024

• Currently, there is **no accurate open-source** DRAM circuit model available to the computer architecture community. This project addresses this gap by providing a reliable DRAM (DDR4) model. I worked on accurately modeling the **data path** from the **DRAM cell to the entire chip**, a critical aspect that is often missing in most architectural studies. We also explored 45, 32, 22 and 16 nm technology nodes.
• Designed an **accurate access transistor** with proper I_{on} and I_{off} currents, addressing existing gaps in DRAM circuit models using **PTM models**. Additionally, we developed a comprehensive DRAM background section that covers data Read/Write paths and timing diagrams as well as performed **energy analysis**.

Publications

[1] S. M. Mojahidul Ahsan, Nouri, **Venkata Ramesh Reddy Ganapam**, Tamzidul Hoque, Mohammad Alian, **"Open-Source DRAM Circuit Model for Future Memory System Exploration" -** *Accepted, ISPASS 2025.*

[2] Ahsan, Nouri, **Venkata Ramesh Reddy Ganapam**, Tamzidul Hoque, Mohammad Alian, **"A Reconfigurable and Accurate Circuit-Level Substrate for DRAM Design and Analysis" -** *Accepted, GLVLSI 2025.*

[3] **Venkata Ramesh Reddy Ganapam**, Sumit Kumar Jha, **"Flow-Based In-memory Computing using a new data structure" -** *Planning to submit, DAC - Nov 2025.*

[4] **Venkata Ramesh Reddy Ganapam**, Sumit Kumar Jha, **"Path-Based In-memory Computing using a new data structure" -** *Planning to submit, ICCAD - Nov 2026.*

Technical Experience

Hardware Design Engineer - Verilog, Matlab - Silicon Labs India Dec 2018 – Jan 2020

• Developed functional and performance test cases, including validation checks for **802.11ax SU, MU, ER,** and **TB** scenarios. Designed and implemented the **FFT** algorithm using the **radix-4**.

• Simulated **802.11ba** Physical layer Tx waveform in MATLAB and Verilog. Modeled the range extension of **BLR 125 kbps Bluetooth** waveform using a **random signal generator** in Matlab. Performed overnight regressions for the Bluetooth physical layer implementations.

Software Developer Intern - C, Python - CISCO Jan 2018 – Jun 2020

• Conducted a white-box **unit testing** and developed test cases in C, as well as **automated test cases** in Python for **CISCO's NRS component** on the Moonshine platform and the **TTY/VTY component** on the CISCO's NCS 5500 platform. Performed overnight sanity simulations for the NRS component.

Selected Projects

Energy and Accuracy Analysis of ML Models Performing Computation Using Analog In-Memory Computing - Cross-sim, C, Python Aug 2024 – Jan 2025

• Conducted a comprehensive **energy** and **accuracy** analysis of the trained model for inference along with the AIMC architecture. Evaluated the accuracy of various **ADC architectures**, including Ramp, SAR, Pipeline, Cyclic, General, and No-ADC architectures. Developed a Python wrapper to calculate **energy consumption**, addressing the lack of energy calculation support in the Cross-sim simulator.

An Open-Source, Accurate Area Model for DDR4 and DDR5 - Python Apr 2024 – Aug 2024

• Developed an area estimation tool for DDR4/DDR5 modules. It calculates the area for **various DRAM architectures** and also accurately calculates the area for these architectures.

Design a Full Adder with Reduced Transmission Delay - Cadence Virtuoso Aug 2016 – Dec 2016

• Designed a full adder using transmission gates with minimal CMOS logic. Analyzed static and dynamic power, completed layout, passed **DRC**, and verified layout-to-schematic equivalence using **LVS**.

Achievements

• Recipient of the **Student Travel Grant** for ISPASS 2023.

• Received **acknowledgment** for the paper "SmartDIMM: In-Memory Acceleration of Upper Layer Protocols" for the circuit model, published in HPCA 2024.

• Received the **MHRD scholarship** and **Teaching Assistantship** during the ME program at BITS Pilani.

Responsibilities

• Teaching Assistant for the courses **Electronics and Digital Circuit Design** and **Introduction to Python** in the Department of Electrical and Computer Engineering at the University of Kansas. Responsible for conducting lab sessions, grading lab sessions, and conducted TA hour sessions.

• Assisted forty students in designing digital and analog circuits on PCBs. Worked with **instruments and electronic devices** such as a Cathode Ray Oscilloscope, Function Generator, Capacitors, Resistors.

• Conducted Python lab sessions for forty students in executing the basic data types, loops, application of the **Numpy, Pandas, Matplotlib** libraries.

Workshop

Non-Traditional Computing with Emerging Technologies for Energy Efficiency - ISSCC Nov 2023

• Future direction of **Processing-in-memory** discussing its advantages and disadvantages.

• Emphasis on the **cross-layer approach** to achieve energy-efficient computing.

• Advancing **Ising accelerator** for Combinatorial Optimization using PIM.